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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/472,869	12/28/1999	Tae-Yong Sohn	Q57124	9316

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EXAMINER	
NATNAEL, PAULOS M	
ART UNIT	**PAPER NUMBER**
2614	

DATE MAILED: 06/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/472,869	SOHN, TAE-YONG	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9 and 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-9 and 11* is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) *3 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1** and **2** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sokawa et al. U.S. Pat. No. 6,353,460 in view of Hwang, U.S. Patent No. 5,896,177.

Considering claim **1,** Sokawa et al discloses the following claimed subject matter, note;

d) a format converter for receiving either of a first input digital signal and a second input digital signal, according to which of the first and second input digital signals is present, the format converter for converting the input digital signal received by the format converter into a predetermined display format output signal, is met by the format conversion section 1100, fig.1;

e) a **controller** for controlling the switching portion to select and output the clock frequency corresponding to a frame rate of the input digital signal, is met by the CPU 1020, fig. 1;

Except for;

a) a first phase locked loop;

b) a second phase locked loop;

c) a switching portion for selecting a clock frequency from one of the first and second phase locked loops according to a predetermined control signal;

Regarding a) and b), Sokawa et al. disclose one PLL circuit. "A clock circuit (not shown) composed of a PLL circuit, for example, for supplying necessary clocks to the respective components of the image processor is also included." (col. 18, lines 32-35) [emphasis added by Examiner]

Hwang discloses a device controlling (and/or converting) an aspect ratio in TV-Monitor integrated wide screen receiver. Specifically, Hwang teaches a phase-locked loop system (Fig.4) wherein a PLL 70, a PLL 80, a multiplier 64, a switch 66 are illustrated. A horizontal sync signal is inputted to the multiplier 64 and the output of the multiplier (2) and the horizontal sync (1) are then input to the switch 66. The output of the switch 66 is inputted to the PLL 70. When the switch 66 selectively outputs a signal to the PLL circuit 70 according to the control signal, PLL 70, as a result, generates at least two different clock frequency signals. (see col. 4, line 23+) Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Sokawa et al by providing the PLL system of Hwang as proposed above, so that the Sokawa system would have the necessary clocks supplied to the components of the image processing circuit according to desired number of such clocks, as suggested by Sokawa in above quoted passage.

Regarding c), the combination of Sokawa et al. and Hwang as modified above in parts (a) and (b) does not disclose a switching means. However, the Examiner takes Official Notice in that it is notoriously well known in the art to utilize a selector or a switching means to select one signal out of a plurality of signals that needs to be processed further, and therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system as proposed above, by providing a switch to select one of the clock signals output from the PLL circuit 70.

Considering claim **2**, the apparatus of claim 1, wherein the first phase locked loop generates a clock frequency of 74.25 MHz, and wherein the second phase locked loop generates a clock frequency of 74.175 MHz.

Regarding claim 2, the combination of Sokawa and Hwang as modified above does not specifically disclose generating a clock frequency of 74.25 MHz and 74.175 MHz for PLL 1 and 2, respectively. However, it would have been an obvious matter of design choice to generate a clock frequency of 74.25 MHz and 74.175 MHz for PLL 1 and 2, or a variation thereof, since Applicant has not disclosed that using a clock frequency of 74.25 MHz and 74.175 MHz for PLL 1 and 2 solves any stated problem or is for any particular purpose and it appears that similar clock frequencies, say, 74.20 MHz or 74.26 MHz, etc. would perform equally well.

Allowable Subject Matter

3. Claims **6-9** and **11** are allowable over the prior art.

4. Claims **3 and 4** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose, a video decoder for decoding a video component of a received digital signal into a first input digital signal, the claimed analog to digital converter for converting a received analog video signal into a second input digital signal, is implied here because the format conversion section is a digital processing device, not an analog processing device. the claimed a format converter for receiving either of a first input digital signal and a second input digital signal, according to which of the first and second input digital signals is present, the format converter for converting the input digital signal into a predetermined display format output signal, the claimed controller for detecting a frame rate of the input digital signal received by said format converter and outputting a timing control signal corresponding to the frame rate detected, the clock frequency providing means for providing a clock frequency according to the timing control signal output by said controller, said clock frequency provided to the format converter for converting the input digital signal received by said format converter into said predetermined display output signal, said clock frequency also provided to said video decoder when said second input digital signal is not present at said format converter; wherein said clock frequency providing means comprises: a first phase

locked loop for generating a first clock frequency; a second phase locked loop for generating a second clock frequency; and a switching portion that receives said timing control signal from said controller and said switching portion outputting one of said first and second clock frequencies corresponding to the received timing control signal as said clock frequency, as in claim 6;

an apparatus selectively converting a clock frequency in a digital signal receiver, comprising: *wherein the input digital signal has a frame rate selected from the group consisting of 60 Hz, 59.94 Hz, 30 Hz, 29.97 Hz, 24 Hz and 23.97 Hz,* wherein if the frame rate of the input digital signal is one of 60 Hz, 30Hz and 24 Hz, the controller controls the switching portion to select and output the clock frequency of the first phase locked loop, *and wherein if the frame rate of the input digital signal is one of 59.94 Hz, 29.97 Hz and 23.97 Hz,* the controller controls the switching portion to select the clock frequency from the second phase locked loop, as in claim **3**;

Response to Arguments

6. Applicant's arguments, see remarks, filed 9-20-04, with respect to claims 1,2,6-9 and 11 have been fully considered and are persuasive. The rejection of claims 6-9 has been withdrawn. Claims 1 and 2 are rejected as shown above.

As to the argument against the motivation to combine references, the applicant is correct; and the motivation to combine has therefore been corrected as shown above in the rejection of claim 1. that is, the reference of Sokawa identifies the need for at least one PLL circuit for supplying necessary clocks to the respective components of the

image processor. Sokawa thus does not preclude having more PLL circuits in order to have enough necessary clocks to components of the system. Therefore, it would be obvious to the skilled in the art to modify and implement the reference of Sokawa in order to have adequately supply clock signals for proper operations of the systems.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (571) 272-7354. The examiner can normally be reached on 10:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (571)272-7353. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN
June 2, 2005

PAULOS M. NATNAEL
PATENT EXAMINER